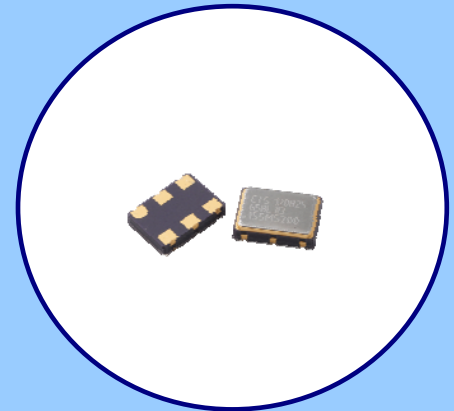


FEATURES

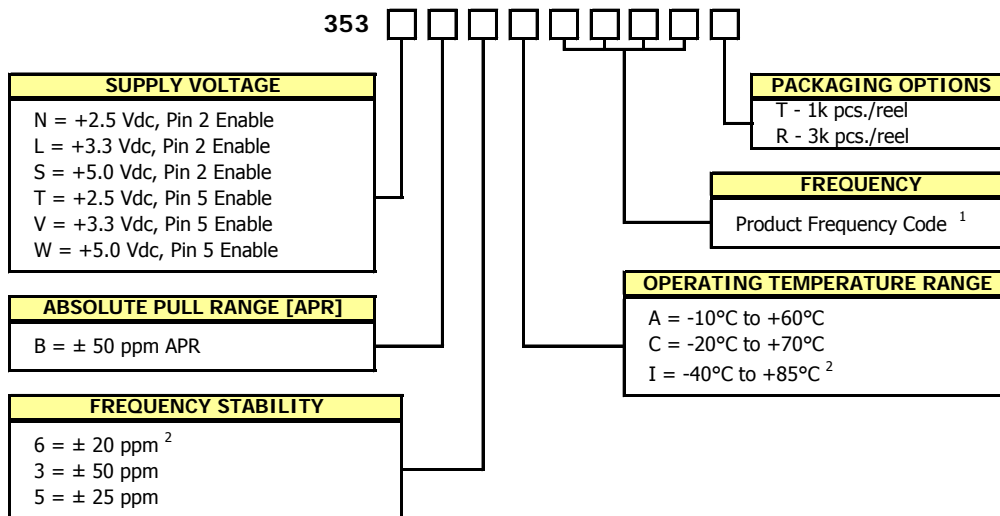
- Standard 5.0mm x 3.2mm 6-Pad Surface Mount Package
- HCMOS Output
- Low Jitter Performance
- Fundamental Crystal Designs
- Frequency Range 1 – 80 MHz
- Operating Voltages +2.5Vdc, +3.3Vdc or +5.0Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



APPLICATIONS

Model 353 is ideal for applications such as broadband access, Ethernet/Gigabit Ethernet, SONET/SDH, xDSL, PCMA, digital video, Picocells and base stations.

ORDERING INFORMATION

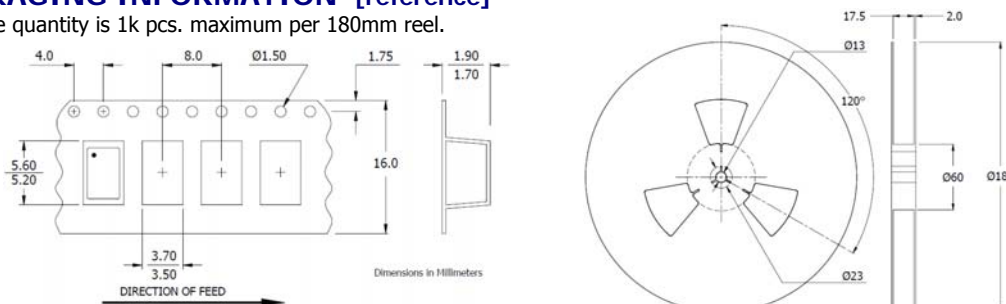


1) Refer to document 016-1454-0, Frequency Code Tables.
3-digits required for frequencies below 100MHz and 4-digits for frequencies 100MHz or greater.
2) Consult factory for availability of 6I Stability/Temperature combination.

**Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.**

PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. maximum per 180mm reel.



ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL PARAMETERS	Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
	Maximum Control Voltage	V_C	-	-0.5	-	V_{CC}	V
	Storage Temperature	T_{STG}	-	-40	-	+100	°C
	Frequency Range	f_o	-	1 - 80			MHz
	Frequency Stability (See Note 1 and Ordering Information)	$\Delta f/f_o$	-	-	-	20, 25 or 50	± ppm
	Absolute Pull Range (See Note 2 and Ordering Information)	APR	-	±50	-	-	ppm
	Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V_{CC} and V_C	-3	-	3	ppm
	Operating Temperature	T_A	-	-10 -20 -40	+25	+60 +70 +86	°C
	Supply Voltage	V_{CC}	Model 353N, 353T, ±5% Model 353L, 353V, ±5% Model 353S, 353W, ±5%	2.38 3.14 4.75	2.5 3.3 5.0	2.63 3.47 5.25	V
	Supply Current	I_{CC}	$C_L = 15$ pF @ +2.5Vdc @ +3.3Vdc @ +5.0Vdc	- - -	- - -	25 25 30	mA
	Output Load	C_L	-	-	-	15	pF
	Control Voltage	V_C	Model 353N, 353T, $V_{CC} = 2.5V$ Model 353L, 353V, $V_{CC} = 3.3V$ Model 353S, 353W, $V_{CC} = 5.0V$	0.20 0.15 0.50	1.25 1.65 2.50	2.30 3.15 4.50	V
	Frequency Deviation	Δf	+25°C @ Time of Shipment, over V_C range	±100	-	-	ppm
	Linearity	L	Best Straight Line Fit	-	-	10	%
	Input Impedance	Z_{Vc}	-	10	-	-	kOhms
	Transfer Function	-	-	Positive			-
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
	Output Voltage Levels	V_{OH} V_{OL}	Logic '1' Level, CMOS Load Logic '0' Level, CMOS Load	$0.9V_{CC}$ -	- -	- $0.1V_{CC}$	V
	Rise and Fall Time	T_{Rr} , T_{Ff}	@ 20%/80% Levels	-	3	8.0	ns
	Start Up Time	T_S	Application of V_{CC}	-	5	10	ms
	Modulation Roll-off	-	@ -3dB	12	-	-	kHz
	Enable Function						
	Enable Input Voltage	V_{IH}	Pin 2 or Pin 5 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
	Disable Input Voltage	V_{IL}	Pin 2 or Pin 5 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	
	Enable Time	T_{PLZ}	Pin 2 or Pin 5 Logic '1'	-	-	100	ns
	Phase Jitter, RMS	t_{jrms}	Bandwidth 12 kHz - 20 MHz	-	0.5	1	ps

1. Notes:

2. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1year aging.

Minimum guaranteed frequency shift from f_o over variations in temperature, aging, power supply and load.

ENABLE TRUTH TABLE

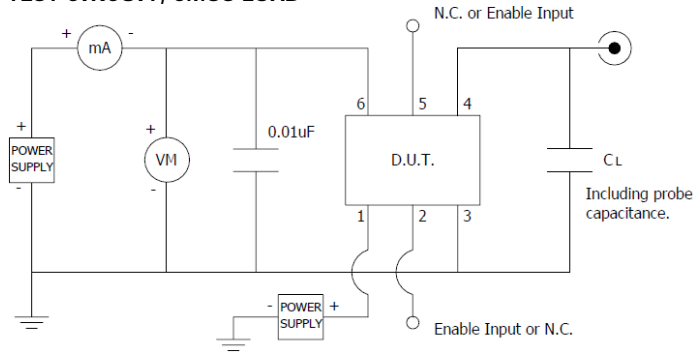
PIN 2 or Pin 5	PIN 4
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

SINGLE SIDE BAND PHASE NOISE
(typical maximum)

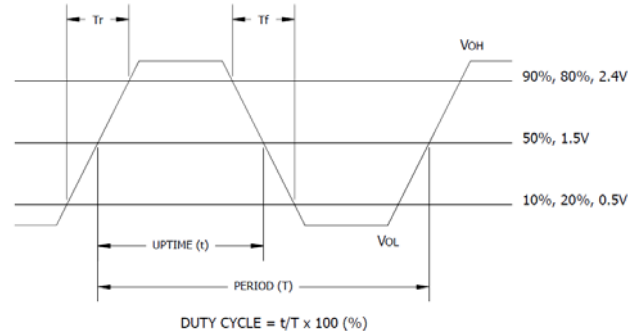
Frequency Offset	Phase Noise (dBc/Hz) *	Frequency Offset	Phase Noise (dBc/Hz) *
10 Hz	-60	10k Hz	-135
100 Hz	-90	100k Hz	-150
1k Hz	-120	>100k Hz	-150

* Results may vary depending on frequency.

TEST CIRCUIT, CMOS LOAD

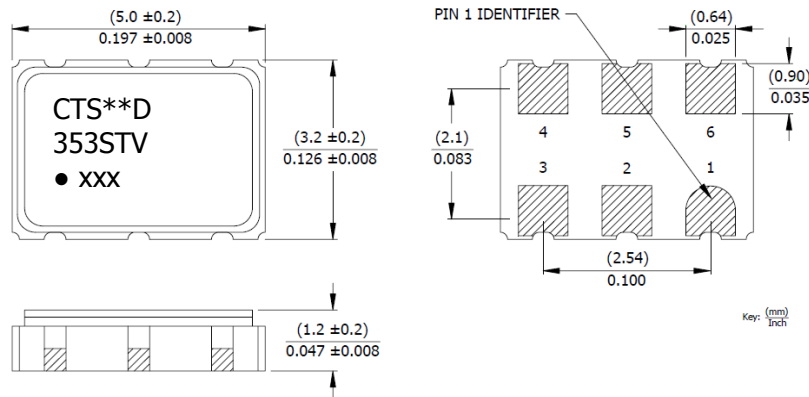


OUTPUT WAVEFORM, CMOS



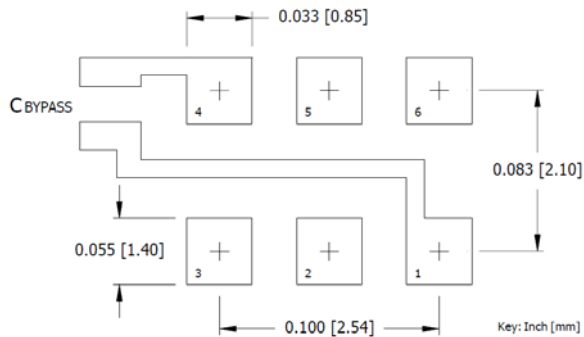
MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.



MARKING INFORMATION

- ** - Manufacturing Site Code.
 - D - Date Code. See Table I for codes.
 - ST - Frequency stability/temperature code. [Refer to Ordering Information.]
 - V - Voltage code. N or T = 2.5V, L or V = 3.3V, S or W = 5.0V
 - xxx - Frequency Code. 3-digits, frequencies below 100MHz
- Refer to document 016-1454-0, Frequency Code Tables.

NOTES

- Complete CTS part number, frequency value and date code information must appear on reel and carton labels.
- Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
- MSL = 1.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	V _C	Control Voltage
2	EOH or N.C.	Enable [std] or No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	N.C. or EOH	No Connect or Enable [opt]
6	V _{CC}	Supply Voltage

TABLE I - DATE CODE

YEAR					MONTH											
2001	2002	2003	2004	2005	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
A	N	a	n	2009	B	P	b	p	2010	C	Q	c	q	2011	D	R
E	S	e	s	2012	F	T	f	t	2013	G	U	g	u	2014	H	V
F	T	f	t	2015	J	W	j	w	2016	K	X	k	x	2017	L	Y
G	U	g	u	2018	M	Z	m	z	2019	N	Y	n	y	2020	O	Z
H	V	h	v	2020	P	Z	p	z								